Fancyyyyy
FCY0006

輪廻転生

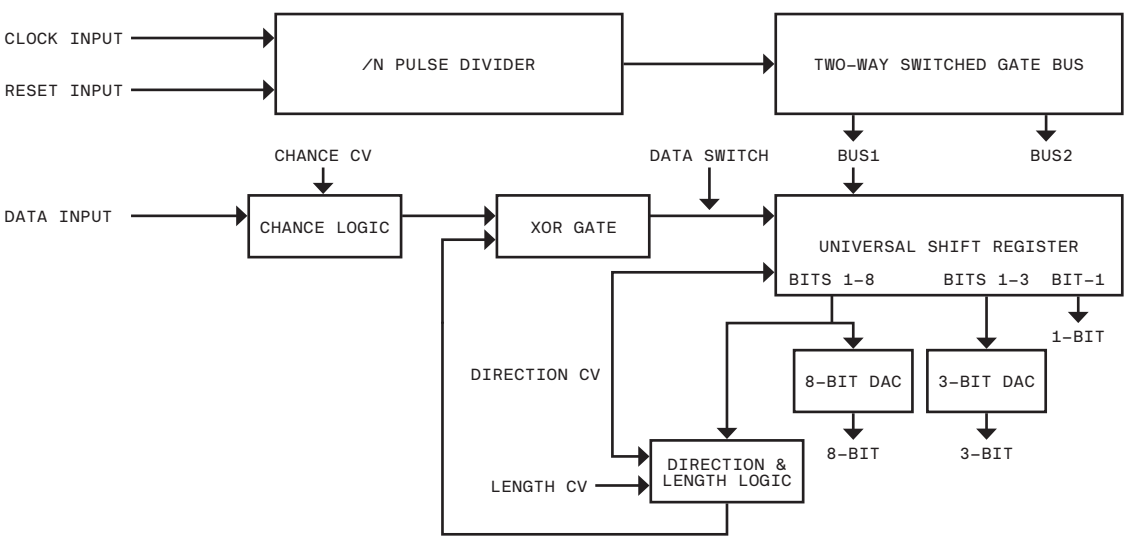
Rung Divisions combines a universal shift register, a “divide by n” pulse divider, analogue noise, and several logic and binary operations. These functions synthesise an array of predictable and unpredictable digital signals at arbitrary time scale.

Rung Divisions’ primary use is as a complex polyrhythmic gate generator that drives a chaotic / pseudo random / looping stepped cv pattern generator, with voltage control over the pattern “direction”, length, and chance of the pattern looping. The combination of these features can be used to generate auditory illusions similar to a stroboscopic effect – like the visual aliasing of a wheel that appears to stand still and reverse direction at speed. Rung Divisions is designed with solid state & discrete logic blocks to work at frequencies between 0–40kHz.

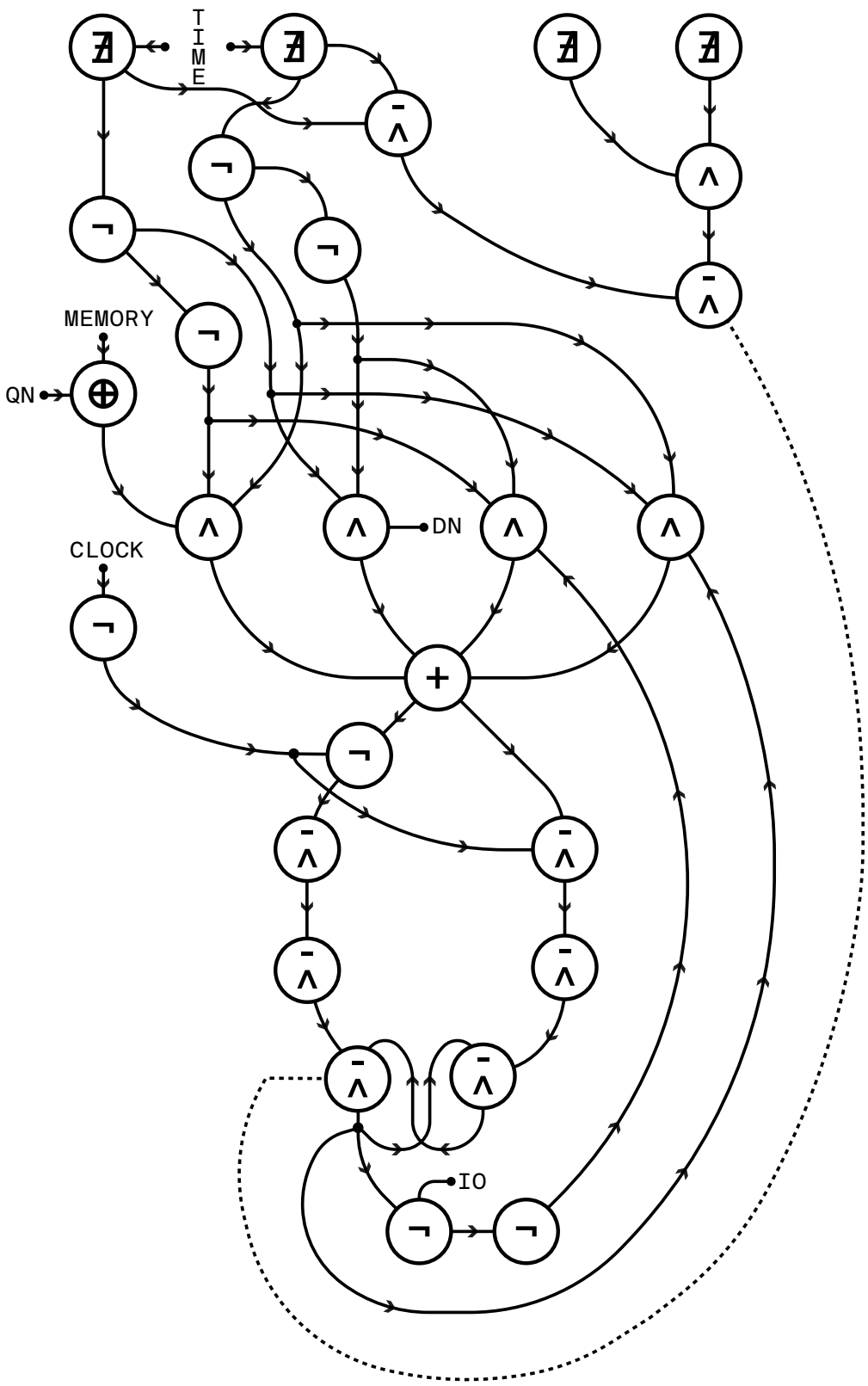
Rung Divisions needs Clock and Data inputs to function, these inputs can be any signal that crosses 1V. The Data input can be taken from the built in Noise source or the clock division outputs. The clock divisions are mixed via OR gates at Bus1 and Bus2, Bus1 clocks the Universal Shift Register. The Data input passes through an XOR gate, the second input for this gate is derived from a complex logic block involving the chance, length, and direction parameters. The Universal Shift Register is encoded to 1-Bit, 3-Bit, and 8-Bit outputs, the 3-Bit and 8-Bit outputs are reverse-encoded for palindromic movement. Feedback to the Clock and Data signal sources adds another layer of complexity to the possible signals generated via these parameters.

Quick Start

- Turn the length knob to “8”. Turn the chance knob fully counterclockwise. Move all switches to the centre position.
- Patch a signal crossing 1V to the clock input. Move the clock switch to the left position. Observe the clock output at Bus1.
- Move the clock switch to the right position. Observe the clock output at Bus2.
- Experiment with moving the clock division switches to the right or left position. Clock divisions are mixed via OR gates at Bus1 or Bus2 according to the switch positions. The shift register is clocked by the signal at Bus1.
- Patch any signal to the Data input and send a clock division to Bus1 by moving its switch to the left position. Data will now enter the shift register according to the signal flow diagram. With chance fully counter-clockwise; an XOR of the data input and the loop point.
- Patch the 3-bit or 8-bit output to the fm input of an oscillator. Observe the oscillator pitch changing according to the data pattern.
- Use the write switch to overwrite high or low data into the shift register.
- Turn the chance knob fully clockwise to lock the pattern in a loop.
- Press the direction button or use a gate signal to reverse the direction of the pattern.
- Turn the length knob or patch a cv to change the length of the looping pattern.
- Turn the chance knob or patch a cv to affect the chance of data coming from the data input, the noise source, or the loop point set by the length and direction parameters.



Polymath
Pulse Divider
Random / Looping Sequencer
Chaotic Signal Generator



- Polyrhythmic Pulse Divider
- Random / Looping Sequencer
- Chaotic Signal Generator
- 12HP
- 128.5 × 60 × 35 mm
- +12V 56mA -12V 41mA

- Graphic design: Joe Gilmore