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User Manual

Fancyyyyy

Contents

Introduction

Rung Divisions consists of several parts: a universal shift register, a “divide by n” pulse divider, dual gate buses, analogue noise, and several logic and binary operations. These functions synthesise an array of predictable and unpredictable digital signals at arbitrary time scale.

Rung Divisions’ primary use is as a complex poly-rhythmic gate generator that drives a chaotic / pseudo random / looping stepped CV pattern generator, with voltage control over the pattern “direction”, length, and chance of the pattern looping.

Rung Divisions v1 was designed and released in 2018 in collaboration with and under license from Rob Hordijk and Ken Stone. The original design impetus was to expand on the complexity of the sequencing and timing outputs of a Benjolin / Rungler in a tactile form factor. This drive came from using a Benjolin as a primary clock and random voltage source in a modular synthesiser. Another objective was to expand on the harmonic complexity of the possible clock and data signals, with the ability to extract lower frequency CV signals from audio rate clock sources. A strength of the Benjolin is how it behaves across the threshold of audio and sub-audio rates, the features of Rung Divisions v1 played to this characteristic.

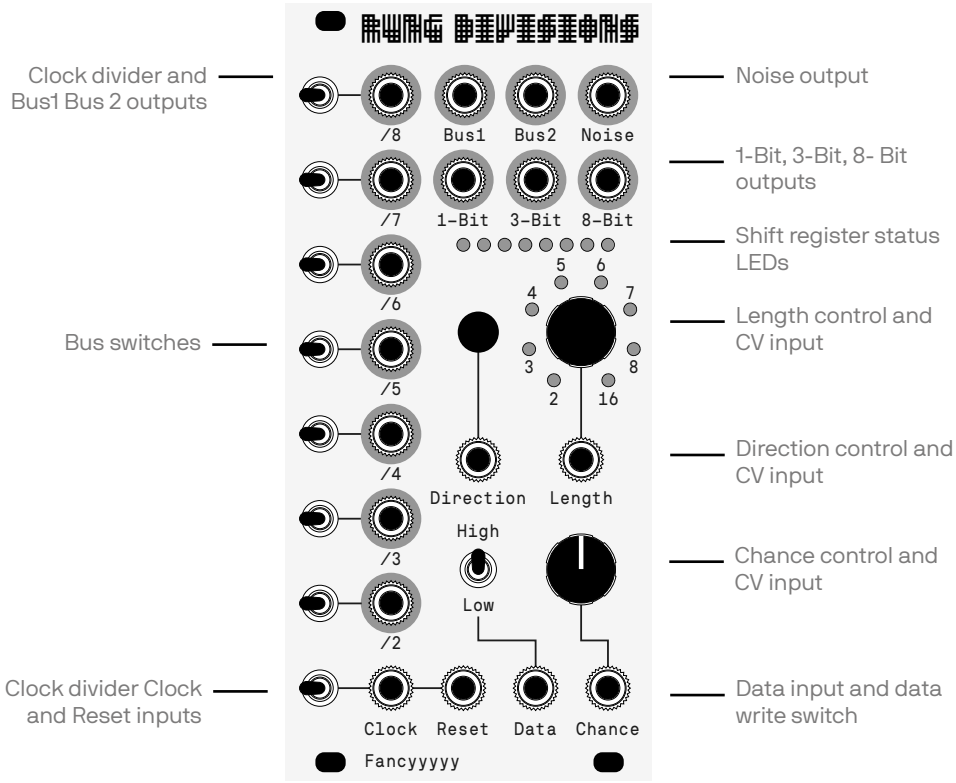
The design has since matured and evolved, Rung Divisions v2 (2023) is a new implementation built around a universal shift register: A universal shift register is a shift register that can shift data to the left or right, allowing the CV output pattern to change “direction”. In addition to this major update, CV control has been added to a number of parameters that generate the stepped CV outputs:

- Pattern Direction CV (trigger input) reverses the pattern read direction
- Loop point CV dynamically modulates the length of the shift register, with a circuit to “flip” the loop points when the pattern changes direction.
- Chance CV controlling the probability of new data entering the shift register.

These new CV controls combine with the poly-rhythmic gate bus to generate patterns in time that shift inside and against one another.

Everything on Rung Divisions can run at audio rates, the module works equally well as a sophisticated sequencing tool and as a complex noise oscillator.

Panel Layout



Technical Specifications:

- Size: 12hp
- Power: +12V 58mA / -12V 42 mA
- Depth: 32mm
- CV Outputs: +/-5V
- Gate Outputs: 0-7V
- Gate Inputs: Clock and Data any signal crossing 1V, Reset and Direction rising edge 700mv minimum
- CV Inputs: Length and Chance +/-5V added to knob position

Clock Division

Rung Divisions has seven integer divide by n pulse dividers. These count the incoming clock pulses and output a pulse every n clocks at divisions between 2 and 8. Fig. 1 shows the timing relationship between the count outputs. The clock input will turn any incoming signal crossing 1V into a pulse to drive the counters - this circuit can be used to derive timing information from complex input signals. The outputs of the counters are fed to eight two input AND gates, with the second input coming from the clock signal - this maintains the pulse width of the incoming clock on all outputs. The clock dividers can run at any frequency between 0 - 40kHz, they can be used to generate poly-rhythms and interrelated clock signals or as sub oscillator / sub-harmonic generators at audio rate. A clock with PWM applied enables dynamic modification of gate output length and harmonically related PWM sounds at audio rate.

A rising edge on the reset input will reset all counts to 0 (and all outputs will go high). /8 will force all outputs to sync to a /7 count making all outputs syncopated, external input to the reset input can generate interesting off-kilter patterns. The count outputs can be used as direction or data inputs, and work well within larger patches as accent gates and clocks for sample and holds.

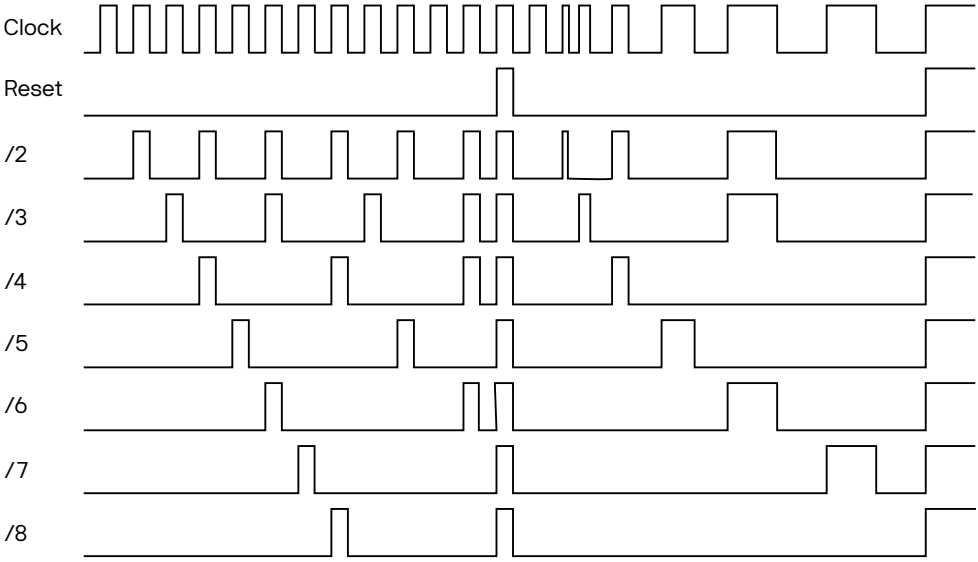


Fig. 1: Clock division timing diagram with reset input

Bus Outputs

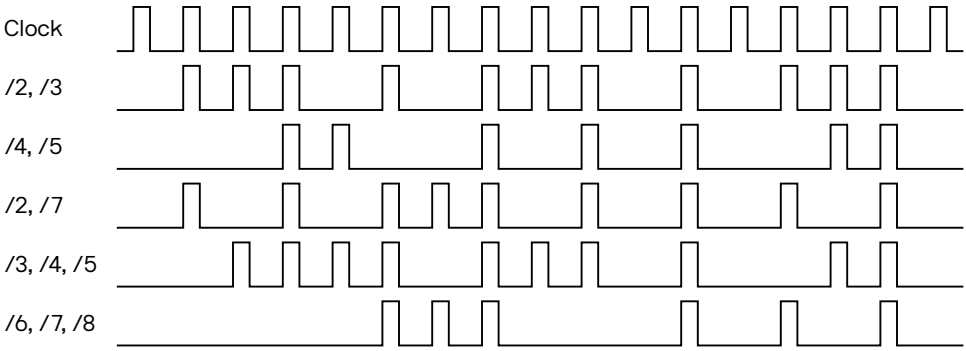


Fig. 2: Timing diagram of various bus output configurations

Clock Divisions can be mixed at the Bus outputs using the eight three-position switches on the left hand side of the module. Put the switch in the left position to send a clock division to Bus1, put the switch in the right position to send a clock division to Bus2.

Poly-rhythmic patterns are easily generated with Rung Divisions through the built in eight input OR gate buses. Mixing clock divisions that do not share a multiplication factor (fig. 2) makes poly-rhythms. Mixing clock divisions that share a multiplication factor (/2, /4 or /3, /6 for example) will have no effect. The Bus outputs also share the pulse width of the incoming clock, and can generate PWM sub-harmonics at audio rates. Organ like tones are also possible when sending the Bus outputs to a tracking low pass filter and changing which sub-harmonics are present in the mix. At sub-audio rates the bus outputs can drive multiple voices or be used as accents.

Prime number divisions behave like an interference pattern as they shift forwards and backwards in time against non prime pulses in a pattern - this effect is audible when listening to the Bus outputs at audio rate - mix /2 and /5, or /7 to hear the interference from the prime count pulses against /2.

Universal Shift Register

The CV outputs from Rung Divisions are generated via a Universal Shift Register. The Universal Shift Register takes its clock from the signal at Bus1. The Data input is derived from the front panel settings:
The loop point (length) of the shift register can be changed under CV, the CV input is added to the knob position.
The read direction of the shift register can be changed by pressing the front panel button or sending a gate into the direction input.
The chance of new data entering the shift register can be controlled under CV, when the knob is fully clockwise the pattern loops, in the counter clockwise position the data comes from an XOR of the front panel data jack and the loop point set by length and direction. The mid position is a noisy interference between the data jack and loop point.

A shift register is a primitive kind of digital memory; the first bit of memory in the register checks its data input every time its clock signal goes high, if the data input is also high at this time, then the first bit of memory stores this high state and waits until the next time the clock goes high. At the next clock high state, the first bit passes it's state onto the next bit in the chain and checks the data input again to update it's own state. In this way, bits of information are passed down the register. A simple way to visualise this is to send a low frequency clock in to Rung Divisions, set the clock switch to the left position to send it to Bus1 and clock the register, set length to "8", set chance fully clockwise, and push the write switch high momentarily. You will see the first led light up of the shift register status display, and the led will shift to the right (or left, depending on the direction setting) at each clock pulse.

When not using the write switch, the data input for the first bit of Rung Divisions is derived from a relatively complex logical block with parameters taken from the chance, length, and direction controls. These two controls set if the data should loop from a loop point, or take new data from the data input on the front panel. All incoming data from the front panel is passed through an XOR gate - this means that the shift register is inherently unstable when data is present at the front panel. Please see fig. 5 signal flow diagram on p.9.

Note that the length parameter changes the loop point regardless of the current state of data in the shift register, it is possible to lose a pattern in situations where data has passed the loop point and the length parameter is changed - for example if you have a length 6 loop and change the loop point when only bit 7 and 8 are high, those two bits of data will be "lost" as they have already passed the loop point.

It is possible to patch a voltage controlled clock divider by looping a sequence, setting 1 bit of data high and using the 1-bit output to clock a sample and hold to update the length parameter at the start of each loop.

CV Outputs

Rung Divisions has three outputs derived from the shift register: a buffered 1-bit gate output from the first bit of the register and two DAC encoded outputs, 3-bit and 8-bit. The 1-bit output maintains the pulse width of the clock signal.

Figs. 3 and 4 show the encoding for the 3-bit and 8-bit outputs - they are reverse encoded and provide contrapuntal motion, which is useful when driving complimentary voices. Changing the direction parameter will make the 3-bit output voltage fall as data passes through the register, and the 8-bit output rise in voltage. Both outputs can serve as a random / looping sequencer and work well with further quantisation.

Due to the extensive CV over the shift register parameters, at audio rate the encoded outputs make for a flexible and comprehensive noise oscillator with as good frequency tracking as the clocking oscillator.

Chaos

To generate chaos with Rung Divisions, the user must patch the 3-bit or 8-bit output back to a CV input of the clock source. Feedback to the data source has less of an impact, but can add an extra layer of control. In a feedback setup, each of the outputs has a distinct character; the 3-bit output is more “burst like” as if there is no data in the last three bits the clock will be held at a slower rate before bursting to higher rates when the data reaches bit 6, 7, and 8. The 8-bit output has a more random character, but will still latch on strange attractors.

The chance knob is especially useful in feedback patches, and can be dialled in to generate slowly changing chaotic patterns.

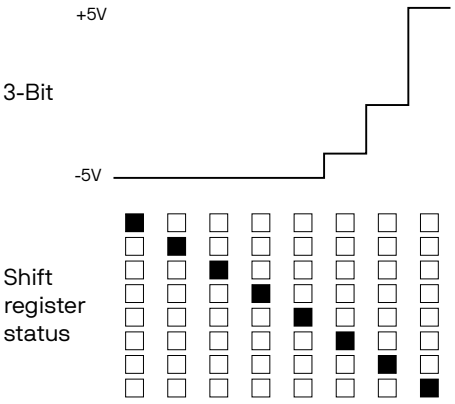


Fig. 3: 3-Bit “rungler” output

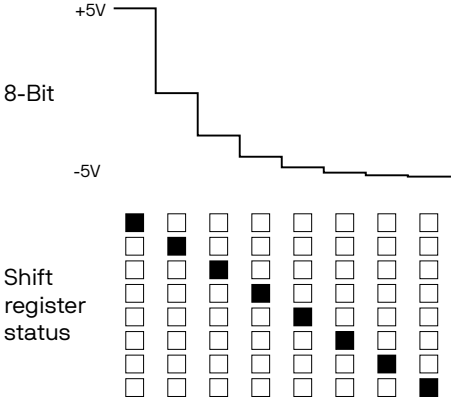


Fig. 4: 8-bit “sequencer” output

Signal Flow Diagram

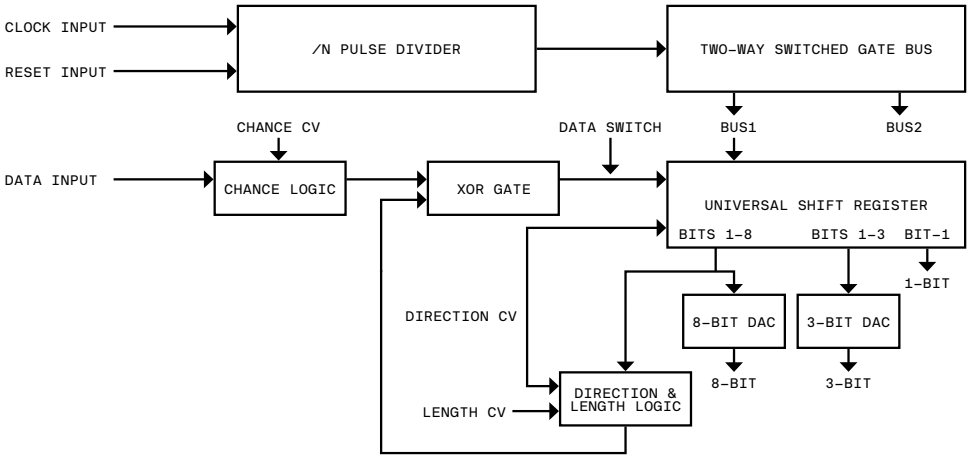


Fig. 5: Signal Flow

Installation and Calibration

Rung Divisions has four pin headers on the rear of the module. Power should only be connected to the pin header labelled “POWER”. Connecting power to any of the other pin headers could irreversibly damage the module. The power header has reverse power protection and should be installed with the red stripe facing down aligned with the mark on the rear PCB.

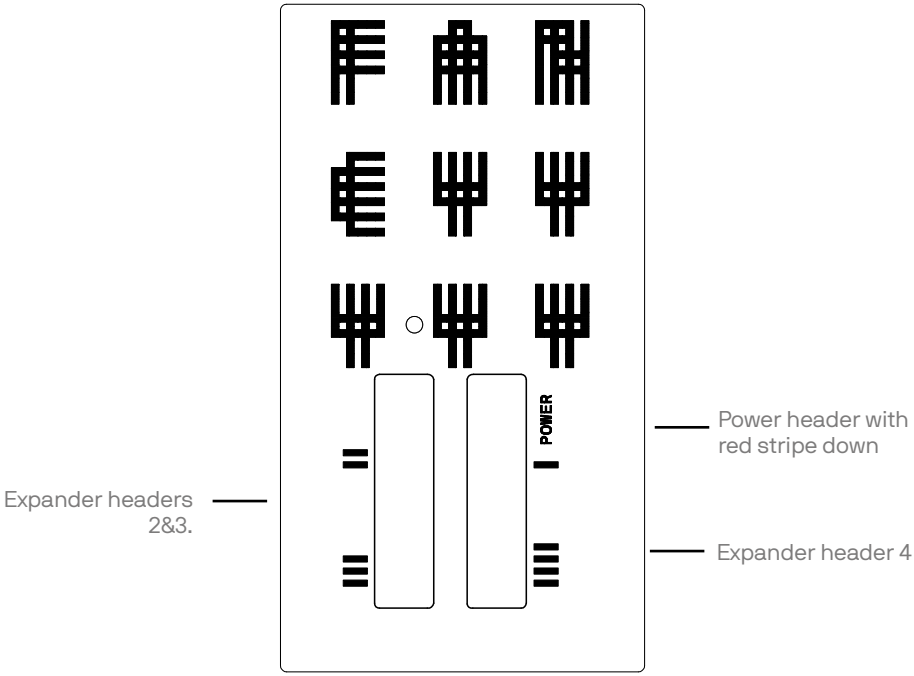


Fig. 6: Rear of module

The trim-pot at the bottom of the module sets the response of the Chance knob and CV. All modules ship calibrated and should not need recalibration. If for some reason you wish to alter the response, send an audio rate clock into Clock, monitor the 8-Bit output, set chance to fully clockwise and turn the trim-pot until the output pattern does not change.

Expanders

Coming soon.

Limited Warranty

From the date of manufacture this device is guaranteed for a period of 2 years against any manufacturing or material defects. Any such defects will be repaired or replaced at the discretion of Fancyyyyy. This does not apply to;

- Physical damage arising for mistreatment (ie dropping, submerging etc).
- Damage caused by incorrect power connections.
- Overexposure to heat or direct sunlight.
- Damage caused by inappropriate or misuse including physical 'modding'.

No responsibility is implied or accepted for harm to person or apparatus caused through operation of this product. By using this product you agree to these terms.

Outside of warranty, please contact info@fancysynthesis.net - we should still be able to help.